Paper ICETIR 2021 Effect of Overlaptime

by Suroso Suroso

Submission date: 05-Apr-2023 12:31PM (UTC+0700)
Submission ID: 2056361704
File name: Published_paper.pdf (1.05M)
Word count: 2132
Character count: 11834

Characteristics of overlap-time effect in a carrier based SPWM three-phase common-emitter CSI

Cite as: AIP Conference Proceedings **2482**, 070003 (2023); https://doi.org/10.1063/5.0110675
Published Online: 21 February 2023

Suroso

Characteristics of Overlap-Time Effect in a Carrier Based SPWM Three-Phase Common-Emitter CSI

Suroso

Author Affiliations
Electrical Engineering Department, Jenderal Soedirman University, Indonesia.

Author Emails
Corresponding author: suroso.te@unsoed.ac.id

Abstract. Overlap-time is appended to the driving signals of current source type inverter to evade open circuit condition of its circuit during operation. However, the overlap-time will cause waveform errors that will affect output waveform quality of inverter circuit. Characteristics and analysis of overlap-time effect were presented and discussed in this paper especially in the three-phase common-emitter current source inverter. Two different carrier based modulation techniques were tested to examine and explore overlap-time effect to the inverter circuit performance. The results showed that by increasing the overlap-time values, the harmonics component of AC output current will increase. Consequently, the waveform distortion will worsen. For different overlap-time values 1 µs to 6 µs, the lowest value of THD was achieved at modulation index 0.9, and the highest THD was occurred at modulation index 1. The data showed that the four-carrier modulation strategy generated lower harmonics content of load current than the two-carrier modulation. Load current harmonics components of the two modulation strategies were less than 2%.

INTRODUCTION

Power inverters are required to change DC power into controllable AC power to meet the load power demand. They are applied such as for photovoltaic (PV) energy conversion where the PV output voltage is a DC voltage, while the load power is AC system. The magnitude, frequency, and phase angle of output voltage or current can be adjusted to meet the application requirements [1, 2]. There are two main inverter topologies, i.e. voltage source inverter and current source inverter circuits. A voltage source inverter works changing the DC input voltage into specified AC voltage. Power capacitors are required as DC energy buffer of inverter circuits. In case of current source power inverter, the inverter proceed the DC input currents become predetermined AC current waveform. In this kind of inverter, power inductor is necessity to generate the DC input current [3-6].

A single-phase power inverter is usually applied for low power application such as in residential photovoltaic system [7-9]. While a three-phase inverter has larger power capacity than a single phase one. Mostly, industrial electrical drives use three-phase inverter system to stir electrical motors in industrial processes [10-12]. A three-phase current source inverter has merits such as better quality of AC current, higher reliability, and fast response of its controller. Hence, considering its features it is interesting to develop this kind of inverter to be applied widely.

Common-emitter current source inverter (CE CSI) is a different inverter circuit developed by author as discussed in [13]. It has advantages related to its common-emitter connection of its controlled power switches. Because of this feature, the gating drive of power switches will be simpler. Moreover, it is more suitable for high frequency operation because of its lower gradient voltage and current during switching operation [14, 15]. More studies are needed to explore characteristics of this inverter circuit. One of them is related to waveform distortion caused by overlap-time in current source inverter topologies [16-19]. Moreover, three-phase circuit configuration of this inverter has not been studied.

The 3rd International Conference on Engineering, Technology and Innovative Researches
AIP Conf. Proc. 2482, 070003-1–070003-6; https://doi.org/10.1063/5.0110675
Published by AIP Publishing. 978-0-7354-4298-6/$30.00

Waveform distortion characteristics of a different configuration of three phase current source inverter was discussed in this paper. Overlap-time effect of its driving control signals was studied. The inverter system with overlap-time was tested by using computer simulation. Some data were presented and discussed in this paper to explore its characteristics.

INVERTER CIRCUITS

Figure 1 (a) presents configuration of a single-phase five-level common-emitter current source inverter. It consists six unidirectional controlled power switches, four power diodes and four DC current sources. All controlled power switches are connected at common point or common emitter terminal. To construct a three-phase inverter configuration, three single phase five-level inverters are connected as shown in Fig. 1 (b). Twelve DC current sources and eighteen unidirectional controlled switches are required in this circuit. However, all of inverter controlled switches are united at common emitter terminal.

The three-phase loads R, S and T in this configuration are connected in Y-connection. Capacitors C_f are connected at output terminal of inverter to output closely sinusoidal output current from the PWM AC current generated by inverter before filtering. The inverter output current is modulated by using carrier based sinusoidal pulse width modulation (SPWM) as represented in Fig. 2. Two modulation strategies are studied for inverter circuits, i.e. four-carrier modulation and two-carrier modulation. The carrier signals are represented by C_1, C_2, C_3 and C_4. The PWM signals generated by modulator circuits are added overlap-time to ensure current paths in the circuit. In practical, it can be realized in both analog and digital circuits.

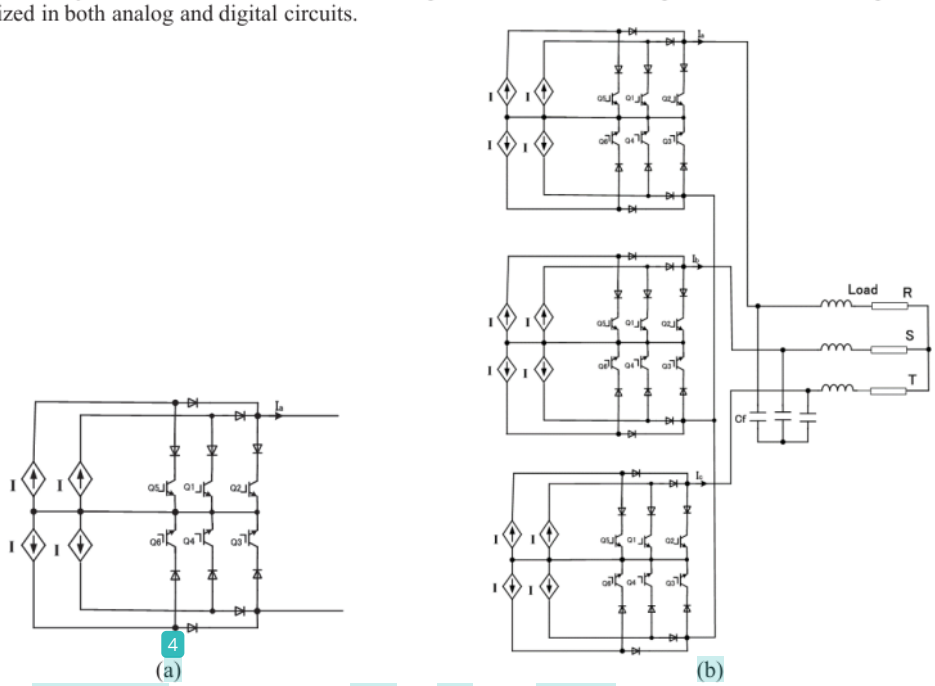

FIGURE 1. (a) Single phase five-level CE CSI [13], (b) Three phase five-level CE CSI

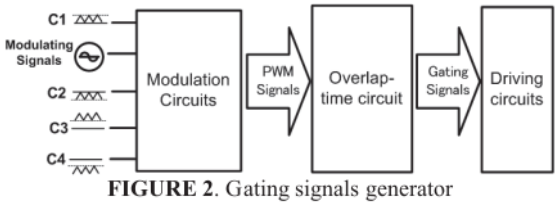

FIGURE 2. Gating signals generator

RESULTS AND ANALYSIS

The inverter circuit was evaluated by computer simulation tests with parameters presented in Table 1. Two modulation techniques were implemented, i.e. two-carrier technique and four-carrier one. Fig. 3 shows the triangular carrier signals for the two-carrier strategy. Moreover, Fig. 4 presents the carrier signals for the four-carrier modulation technique. The frequency of these carrier signals was set the same as 20 kHz, with output current frequency 50 Hz. The gating signals were added various overlap-time values, i. e. 1 µs, 2 µs, 3 µs, 4 µs, 5 µs, and 6 µs. Fig. 5 shows two gating signals of inverter's switches added with 2 µs overlap-time. The two signals overlapped each other for 2 µs that make continuous current paths in inverter circuit. The inverter was connected to power load resistor R=1 Ω, and inductor L=0.1 mH. Capacitor filter 200 µF was applied at inverter output terminal to filter harmonics of PWM current produced by inverter.

TABLE 1. Inverter circuit parameters

Parameters	Value
DC current source	10 A
Switching speed	20 kHz
Main frequency	50 Hz
Overlap time values	1 µs, 2 µs, 3 µs, 4 µs, 5 µs, 6 µs
Filter C_f	200 µF
Load/phase	R=1 Ω, L=0.1 mH

Load current waveforms of the inverter are depicted in Fig. 6. Three-phase sinusoidal load current flown thru the power load. Moreover, the five-level PWM current can also be observed in this figure. The measured data depicting relation between overlap-time grades and total harmonics distortion (THD) of load current for distinct modulation strategy is presented in Fig. 7. and Fig. 8. The graph trend shows that by enlarging the overlap-time, the waveform distortion will also escalate. For different overlap-time values, the lowest value of THD was achieved at modulation index 0.9, and the highest THD was occurred at modulation index 1. Harmonics spectra of load current at modulation index (MI) 0.9 for two-carrier modulation strategy is shown in Fig. 9. Harmonics components were less than 2%. Moreover, harmonics spectra for four-carrier modulation technique at modulation index (MI) 0.9 is presented in Fig. 10. The data show that the four-carrier modulation strategy generated lower harmonics content of load current.

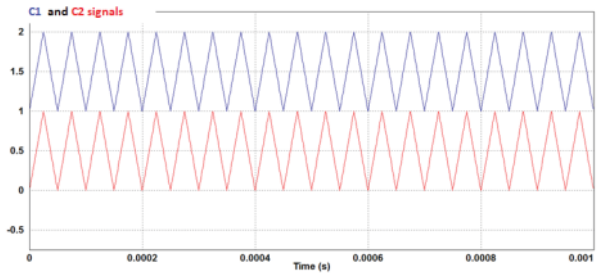

FIGURE 3. Two carrier signals of PWM modulation [14]

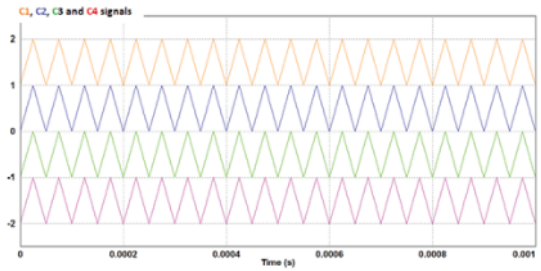

FIGURE 4. Four carrier signals of PWM modulation [13, 15]

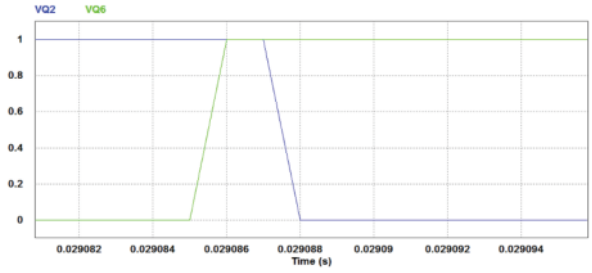

FIGURE 5. Overlap-time 2 μs between switch Q_2 and Q_6

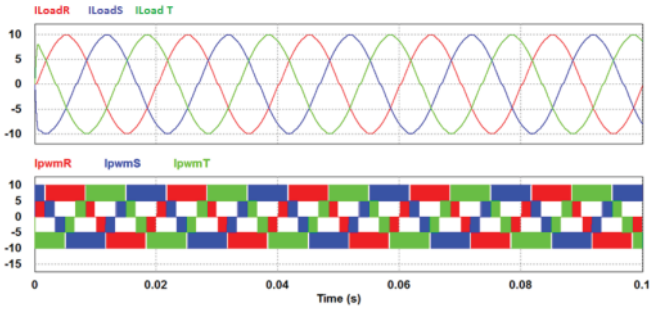

FIGURE 6. Load current and five-level current waveforms

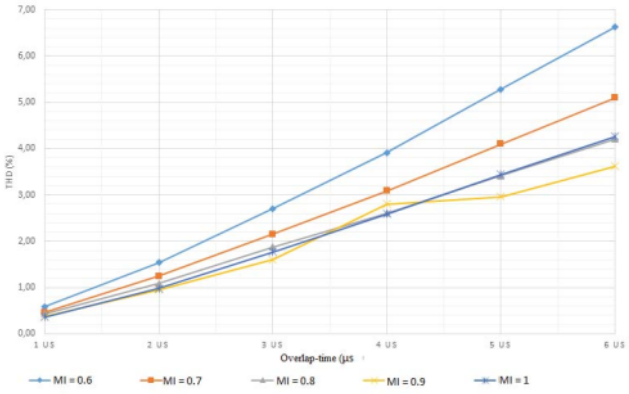

FIGURE 7. Relation between THD and overlap-time values for two carrier modulation

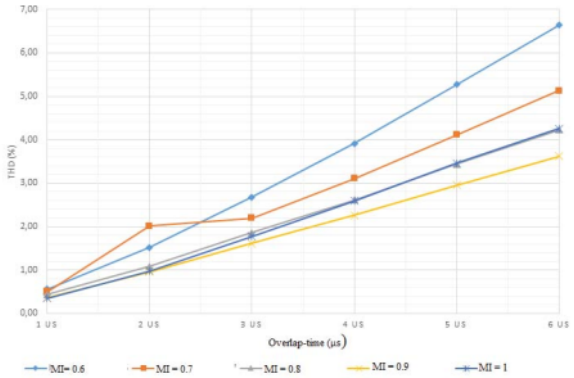

FIGURE 8. Relation between THD and overlap-time values for four-carrier modulation

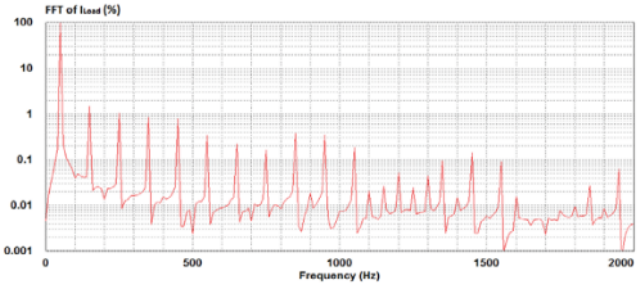

FIGURE 9. Harmonics spectra of load current at MI= 0.9 for two-carrier modulation

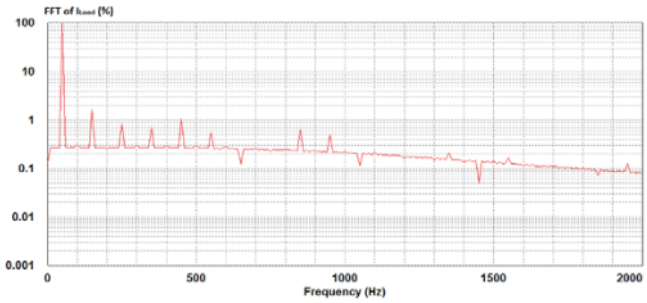

FIGURE 10. Harmonics spectra of load current at MI=0.9 for four carrier modulation

CONCLUSIONS

Configuration of different three phase current source inverter circuit applying common-emitter configuration of its controlled power switches was presented in this paper. The quality of its output current waveform was investigated and examined regarding the adding of overlap-time in its driving signals. The results showed that the distortion of inverter's output current and voltage will increase if the overlap-time value is increased. For different overlap-time values between 1 µs to 6 µs, the lowest value of THD was achieved at modulation index 0.9, and the highest THD was occurred at modulation index 1. The data showed that the four-carrier modulation strategy generated lower harmonics content of load current than the two-carrier modulation. Minimizing the overlap-time effect is a mandatory to achieve high quality output power of a current source power inverter.

ACKNOWLEDGMENTS

This study was funded by research grant provided by Jenderal Soedirman University, Indonesia.

REFERENCES

1. J. Rodiguez, J. S. Lai, , and F. Z. Peng, "Multilevel inverter: a survey of topologies, controls, and application", *IEEE Transactions on Industrial Electronics*, vol. 49, no.4, pp. 724-738, 2002.
2. Z H. Bai, and Z. C. Zhang, "Conformation of multilevel current source converter topologies using the duality principle," *IEEE Transactions on Power Electronics*, vol. 23, no. 5, pp. 2260-2267, 2008.
3. Suroso, D. T. Nugroho, and T. Noguchi, "A nine-level hybrid current source inverter using common-emitter topology and inductor-cell", *International Journal of Power Electronics and Drive Systems*, vol. 10, no. 2, pp. 852-859, 2019.
4. Suroso, Winasis, and T. Noguchi, "Overlap-time compensation technique for current-source power inverter", *IET Power Electronics*, vol. 13, no.4, pp. 854-862, 2020.
5. T. Noguchi, and Suroso, "Review of novel multilevel current-source inverters with H-bridge and common-emitter based topologies", Proc. of IEEE Energy Conversion Congress and Exposition, 2010, pp. 4006-4011.
6. L. S. Garcia, H. J. Avelar, L. C. de Freitas, and J.B. Vieira, "Evaluation of a single-stage current source inverter with high voltage gain supplied by a PEM fuel cell", *IET Power Electronics*, vol. 5, no. 9, pp. 1–13, 2012.
7. Z. Wang, L. Jiang, Z. Zou, and M. Cheng, "Operation of SMES for the current source inverter fed distributed power system under islanding mode", *IEEE Transactions Applied Superconductivity*, vol. 23, no.3, pp. 5700404-5700404, 2013
8. C. R. Baier, M. A. Torres, P. Acuna, J. A. Muñoz, P. E. Melín, and C. Restre, "Analysis and design of a control strategy for tracking sinusoidal references in single-phase grid-connected current-source inverters", *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 819-832, 2018.
9. L. S. Garcia, G. M. Buiatti, L. C. de Freitas, and E. A. A. Coelho, "Dual transformerless single-stage current source inverter with energy management control strategy", *IEEE Transactions on Power Electronics*, vol. 28, no.10, pp. 4644-4656, 2013.
10. B. Wu, J. Pontt, J. Rodriguez, S. Bernet, and S. Kouro, "Current-source converter and cycloconverter topologies for industrial medium-voltage drives", *IEEE Transactions Industrial Electronics*, vol. 55, no.7, pp. 2786-2797, 2008.
11. S. Kouro, J. Rodriguez, B. Wu, S. Bernet, and M. Perez, "Powering the future of industry: high-power adjustable speed drive topologies", *IEEE Industry Application Magazine*, vol. 18, no.4, pp. 26-39, 2012.
12. T. Halkosaari, K. Kuusel, and H. Tuusa, "Effect of non-idealities on the performance of the 3-phase current source PWM converter", Proc. of IEEE 32nd Annual Power Electronics Specialists Conference, 2001, pp. 654-659.
13. Suroso, and T. Noguchi, "Common-emitter topology of multilevel current-source pulse width modulation inverter with chopper-based DC current sources", *IET Power Electronics*, vol. 4, no. 7, pp. 759-766, 2011.
14. T. Noguchi, and Suroso, "New multilevel current source PWM inverter with full-bridge inductor cells", *IEEJ Transactions on Industry Applications,* vol. 130, no.6, pp. 808-815, 2010.
15. Suroso, Winasis, and T. Noguchi, "Overlap-time compensation technique for current-source power inverter", *IET Power Electronics*, vol. 13, iss. 4, pp. 854-862, 2020.
16. H. Qin, Q. Liu, X. Zhang, Y. Zhang and D. Wang, D., "Influence of the overlap time on the ac grid current of CSR and its restraining method", Proc. of IECON, 2017, pp. 1249-1254
17. A. Akdag, P. Stefanutti, L. Meysenc and N. Hugo, "Overlap time and voltage drop compensation in an AC/AC converter", Proc. of 38th IAS Annual Meeting on Conference Record of the Industry Applications Conference, 2003, pp. 205-212
18. Y. Geng, R. Deng, W. Dong, K. Wang, H. Liu, and X. Wu, "An overlap-time compensation method for current-source space-vector PWM inverters", *IEEE Transactions on Power Electronics*, vol. 33, no.4 , pp. 3192 – 3203, 2018.
19. H. Qin, Q. Liu, Q., Y. Zhang, X. Zhang, and D. Wang, "A new overlap current restraining method for current-source rectifier", *Journal of Power Electronics*, vol. 18, no. 2, pp. 615-626, 2018.

Paper ICETIR 2021 Effect of Overlaptime

ORIGINALITY REPORT

22%	13%	16%	4%
SIMILARITY INDEX	INTERNET SOURCES	PUBLICATIONS	STUDENT PAPERS

PRIMARY SOURCES

1	Submitted to Universitas Jenderal Soedirman Student Paper	3%
2	Suroso, Hari Siswantoro. "Characteristics of DC current component injection in grid tied H-bridge CSI with transformer", AIP Publishing, 2023 Publication	3%
3	Suroso, Winasis, Toshihiko Noguchi. "Overlap-time compensation technique for current-source power inverter", IET Power Electronics, 2020 Publication	2%
4	telkomnika.uad.ac.id Internet Source	2%
5	docplayer.fr Internet Source	2%
6	tii.ieee-ies.org Internet Source	2%
7	jestec.taylors.edu.my Internet Source	1%

8	pdfs.semanticscholar.org Internet Source	1 %
9	ijpeds.iaescore.com Internet Source	1 %
10	Noguchi, Toshihiko, and Suroso. "Review of novel multilevel current-source inverters with H-bridge and common-emitter based topologies", 2010 IEEE Energy Conversion Congress and Exposition, 2010. Publication	1 %
11	Suroso Suroso, Hari Siswantoro. "Study of novel parallel H-bridge and common-emitter current-source inverters for photovoltaic power conversion system", International Journal of Power Electronics and Drive Systems (IJPEDS), 2022 Publication	1 %
12	Suroso. "A new three-level current-source PWM inverter and its application for grid connected power conditioner", Energy Conversion and Management, 201007 Publication	1 %
13	Mahmoud G. Sayed, Omar Abdel-Rahim, M. Orabi. "Comparative Study to Investigate the Effect of Five VS Seven Segment Modulation Sequence on the Waveform Distortion Resulted by the Overlap Time in Current	1 %

Source Inverter", 2019 International Conference on Innovative Trends in Computer Engineering (ITCE), 2019
Publication

14	digital-library.theiet.org Internet Source	1 %
15	www.bartleby.com Internet Source	1 %
16	www.ijrsm.com Internet Source	1 %
17	Suroso, Daru Tri Nugroho, Winasis. "A three-level common-emitter current source inverter with reduced device count", 2017 4th International Conference on Information Technology, Computer, and Electrical Engineering (ICITACEE), 2017 Publication	1 %
18	www.researchgate.net Internet Source	1 %
19	Hao Ding, Xiaoqiang Guo, Meiling He, Changli Shi, Dongqiang Jia, Chao Chen, Josep M. Guerrero. "A New Modulation to Eliminate the Impact of Overlap Time for Three-Phase Current Source Converters", Journal of Electrical Engineering & Technology, 2022 Publication	<1 %

Exclude quotes	On	Exclude matches	Off
Exclude bibliography	On		