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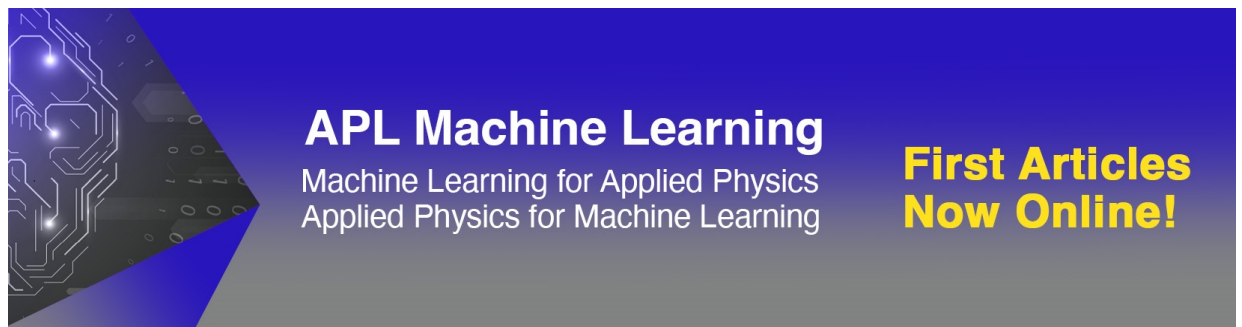
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# Characteristics of Overlap-Time Effect in a Carrier Based SPWM Three-Phase Common-Emitter CSI

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**Abstract.** Overlap-time is appended to the driving signals of current source type inverter to evade open circuit condition of its circuit during operation. However, the overlap-time will cause waveform errors that will affect output waveform quality of inverter circuit. Characteristics and analysis of overlap-time effect were presented and discussed in this paper especially in the three-phase common-emitter current source inverter. Two different carrier based modulation techniques were tested to examine and explore overlap-time effect to the inverter circuit performance. The results showed that by increasing the overlap-time values, the harmonics component of AC output current will increase. Consequently, the waveform distortion will worsen. For different overlap-time values 1  $\mu$ s to 6  $\mu$ s, the lowest value of THD was achieved at modulation index 0.9, and the highest THD was occurred at modulation index 1. The data showed that the four-carrier modulation strategy generated lower harmonics content of load current than the two-carrier modulation. Load current harmonics components of the two modulation strategies were less than 2%.

## INTRODUCTION

Power inverters are required to change DC power into controllable AC power to meet the load power demand. They are applied such as for photovoltaic (PV) energy conversion where the PV output voltage is a DC voltage, while the load power is AC system. The magnitude, frequency, and phase angle of output voltage or current can be adjusted to meet the application requirement [1, 2]. There are two main inverter topologies, i.e. voltage source inverter and current source inverter circuits. A voltage source inverter works changing the DC input voltage into specified AC voltage. Power capacitors are required as DC energy buffer of inverter circuits. In case of current source power inverter, the inverter proceed the DC input currents become predetermined AC current waveform. In this kind of inverter, power inductor is necessity to generate the DC input current [3-6].

A single-phase power inverter is usually applied for low power application such as in residential photovoltaic system [7-9]. While a three-phase inverter has larger power capacity than a single phase one. Mostly, industrial electrical drives use three-phase inverter system to stir electrical motors in industrial processes [10-12]. A three-phase current source inverter has merits such as better quality of AC current, higher reliability, and fast response of its controller. Hence, considering its features it is interesting to develop this kind of inverter to be applied widely.

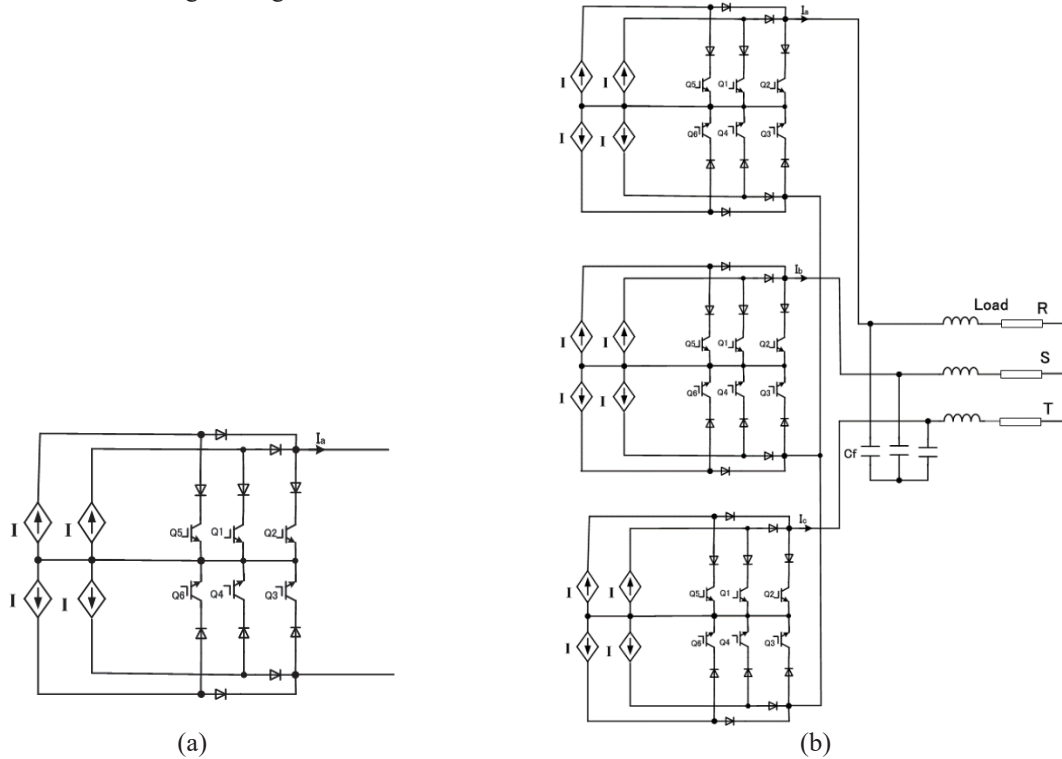
Common-emitter current source inverter (CE CSI) is a different inverter circuit developed by author as discussed in [13]. It has advantages related to its common-emitter connection of its controlled power switches. Because of this feature, the gating drive of power switches will be simpler. Moreover, it is more suitable for high frequency operation because of its lower gradient voltage and current during switching operation [14, 15]. More studies are needed to explore characteristics of this inverter circuit. One of them is related to waveform distortion caused by overlap-time in current source inverter topologies [16-19]. Moreover, three-phase circuit configuration of this inverter has not been studied.

Waveform distortion characteristics of a different configuration of three phase current source inverter was discussed in this paper. Overlap-time effect of its driving control signals was studied. The inverter system with overlap-time was tested by using computer simulation. Some data were presented and discussed in this paper to explore its characteristics.

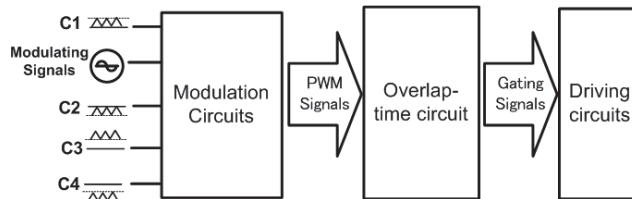
## INVERTER CIRCUITS

Figure 1 (a) presents configuration of a single-phase five-level common-emitter current source inverter. It consists six unidirectional controlled power switches, four power diodes and four DC current sources. All controlled power switches are connected at common point or common emitter terminal. To construct a three-phase inverter configuration, three single phase five-level inverters are connected as shown in Fig. 1 (b). Twelve DC current sources and eighteen unidirectional controlled switches are required in this circuit. However, all of inverter controlled switches are united at common emitter terminal.

The three-phase loads R, S and T in this configuration are connected in Y-connection. Capacitors  $C_f$  are connected at output terminal of inverter to output closely sinusoidal output current from the PWM AC current generated by inverter before filtering. The inverter output current is modulated by using carrier based sinusoidal pulse width modulation (SPWM) as represented in Fig. 2. Two modulation strategies are studied for inverter circuits, i.e. four-carrier modulation and two-carrier modulation. The carrier signals are represented by  $C_1$ ,  $C_2$ ,  $C_3$  and  $C_4$ . The PWM signals generated by modulator circuits are added overlap-time to ensure current paths in the circuit. In practical, it can be realized in both analog and digital circuits.



**FIGURE 1.** (a) Single phase five-level CE CSI [13], (b) Three phase five-level CE CSI



**FIGURE 2.** Gating signals generator

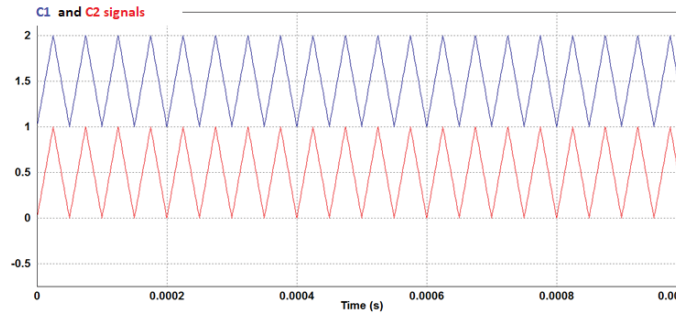
## RESULTS AND ANALYSIS

The inverter circuit was evaluated by computer simulation tests with parameters presented in Table 1. Two modulation techniques were implemented, i.e. two-carrier technique and four-carrier one. Fig. 3 shows the triangular carrier signals for the two-carrier strategy. Moreover, Fig. 4 presents the carrier signals for the four-carrier modulation technique. The frequency of these carrier signals was set the same as 20 kHz, with output current frequency 50 Hz. The gating signals were added various overlap-time values, i. e. 1  $\mu$ s, 2  $\mu$ s, 3  $\mu$ s, 4  $\mu$ s, 5  $\mu$ s, and 6  $\mu$ s. Fig. 5 shows two gating signals of inverter's switches added with 2  $\mu$ s overlap-time. The two signals overlapped each other for 2  $\mu$ s that make continuous current paths in inverter circuit. The inverter was connected to power load resistor  $R=1\ \Omega$ , and inductor  $L=0.1\text{ mH}$ . Capacitor filter 200  $\mu$ F was applied at inverter output terminal to filter harmonics of PWM current produced by inverter.

**TABLE 1.** Inverter circuit parameters

Parameters	Value
DC current source	10 A
Switching speed	20 kHz
Main frequency	50 Hz
Overlap time values	1 $\mu$ s, 2 $\mu$ s, 3 $\mu$ s, 4 $\mu$ s, 5 $\mu$ s, 6 $\mu$ s
Filter $C_f$	200 $\mu$ F
Load/phase	$R=1\ \Omega$ , $L=0.1\text{ mH}$

Load current waveforms of the inverter are depicted in Fig. 6. Three-phase sinusoidal load current flown thru the power load. Moreover, the five-level PWM current can also be observed in this figure. The measured data depicting relation between overlap-time grades and total harmonics distortion (THD) of load current for distinct modulation strategy is presented in Fig. 7. and Fig. 8. The graph trend shows that by enlarging the overlap-time, the waveform distortion will also escalate. For different overlap-time values, the lowest value of THD was achieved at modulation index 0.9, and the highest THD was occurred at modulation index 1. Harmonics spectra of load current at modulation index (MI) 0.9 for two-carrier modulation strategy is shown in Fig. 9. Harmonics components were less than 2%. Moreover, harmonics spectra for four-carrier modulation technique at modulation index (MI) 0.9 is presented in Fig. 10. The data show that the four-carrier modulation strategy generated lower harmonics content of load current.



**FIGURE 3.** Two carrier signals of PWM modulation [14]

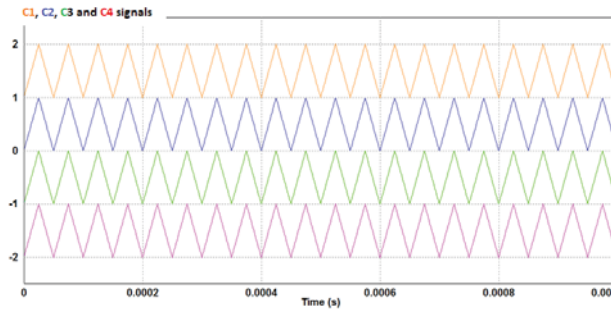


FIGURE 4. Four carrier signals of PWM modulation [13, 15]

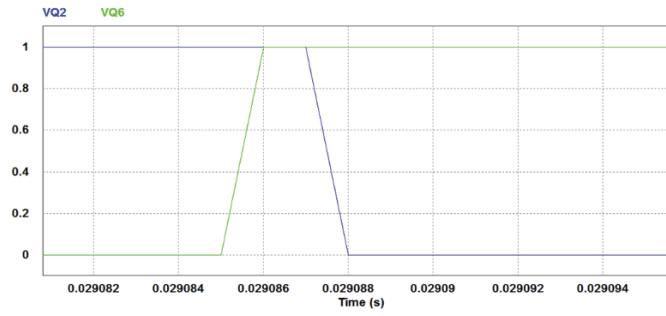


FIGURE 5. Overlap-time 2  $\mu$ s between switch  $Q_2$  and  $Q_6$

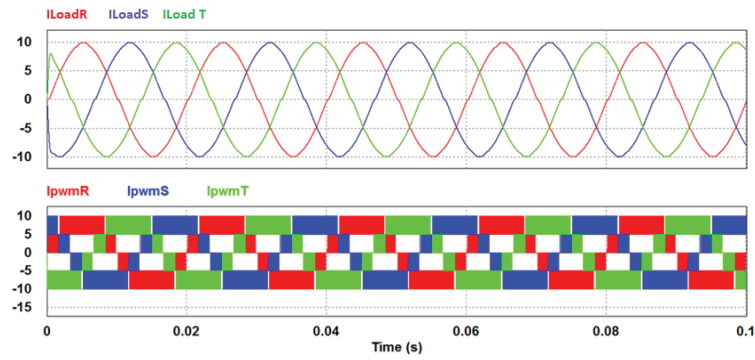


FIGURE 6. Load current and five-level current waveforms

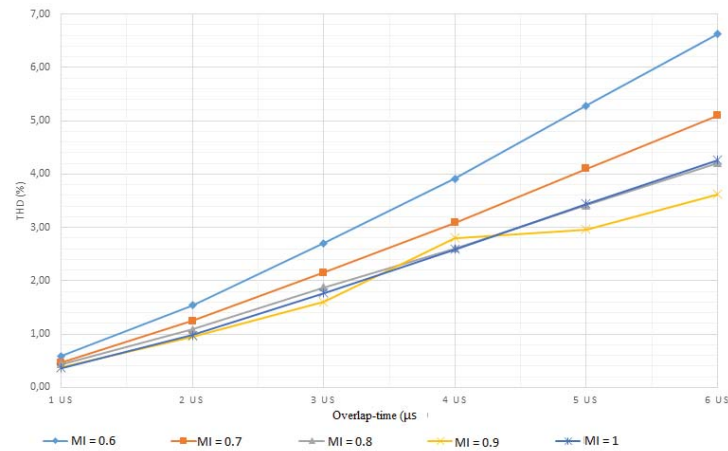
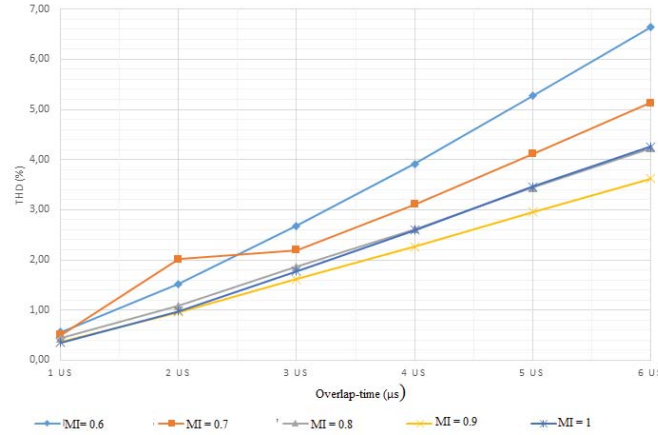
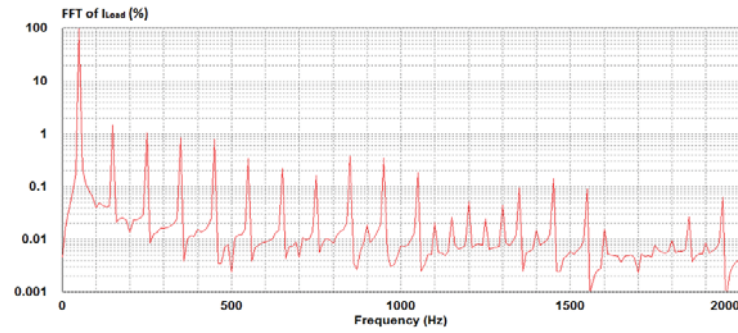


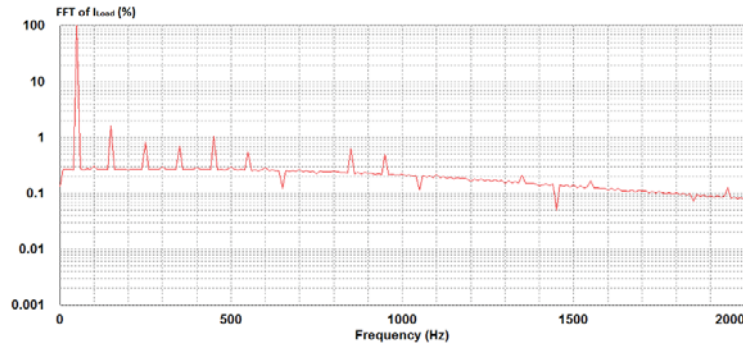
FIGURE 7. Relation between THD and overlap-time values for two carrier modulation



**FIGURE 8.** Relation between THD and overlap-time values for four-carrier modulation



**FIGURE 9.** Harmonics spectra of load current at MI= 0.9 for two-carrier modulation



**FIGURE 10.** Harmonics spectra of load current at MI=0.9 for four carrier modulation

## CONCLUSIONS

Configuration of different three-phase current source inverter circuit applying common-emitter configuration of its controlled power switches was presented in this paper. The quality of its output current waveform was investigated and examined regarding the adding of overlap-time in its driving signals. The results showed that the distortion of inverter's output current and voltage will increase if the overlap-time value is increased. For different overlap-time values between 1  $\mu$ s to 6  $\mu$ s, the lowest value of THD was achieved at modulation index 0.9, and the highest THD was occurred at modulation index 1. The data showed that the four-carrier modulation strategy generated lower harmonics content of load current than the two-carrier modulation. Minimizing the overlap-time effect is a mandatory to achieve high quality output power of a current source power inverter.

## ACKNOWLEDGMENTS

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